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09/728,022  
Examiner: T. R. Sundaram

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<u>L2</u>	L1 and multiplexer and memory	71	<u>L2</u>
<u>L1</u>	integrated ADJ circuit with test\$3 and (test or mask) with vector and (deterministic or pseudo with random)	166	<u>L1</u>

END OF SEARCH HISTORY